ANNA UNIVERSITY COIMBATORE

B.E.I B.TECH. DEGREE EXAMINATIONS: MAY / JUNE 2010

REGULATIONS: 2007

THIRD SEMESTER

070230011 - COMPUTER ARCHITECTURE

(COMMON TO CSE *IiT*)

TIME: 3 Hours **Max.Marks: 100**

PART-A **(20 x 2 = 40 MARKS)**

ANSWER ALL QUESTIONS

1. Define the working of **MAR** and MDR.
2. What are the addressing modes used for Branching instruction?
3. How an execution time of a program is calculated.
4. Define the two different Byte addressing methods.
5. Draw the full adder circuit using two half adders and give the truth table.
6. How does Booth algorithm helps for Arithmetic calculations?
7. What are guard bits?
8. Write the various ways of representing signed integer in the system.
9. Draw the basic organization of micro programmed control unit.
10. What is Wide branch addressing?
11. What is a pipeline hazard?
12. Give the structure of two stage instruction pipeline.
13. Draw the organization of CMOS memory cell.
14. Write note on Cache memory.
15. Define hit and miss rate?
16. What is data striping?
17. How device identification is performed on interrupts.
18. Define vector interrupts.

19. List the functions of I/O interface.

20. Draw the structure of two channel DMA controller.

PART - B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. a) Explain various assembler directives used in assembly language program. 6

    b) Discuss the various Instruction types. 6

22. With a neat sketch, Explain in detail about logic design for fast adders.

23. With a neat block diagram, explain in detail about micro programmed control unit and explain its operations.

24. a) Explain the concept of virtual memory with anyone virtual memory 6 management technique.

    b) Discuss any six ways of improving the cache performance. 6

25. Explain in detail about interrupt handling.

26. Describe in detail about pipeline processing

27. What is Memory Interleaving? Explain the addressing of multiple modules memory system.

28. Explain the use of vectored interrupts in processes. Why is priority handling desired in interrupt controllers? How does the different priority scheme work? *****THE END*****